Amendments to the Claims

1. (withdrawn) A semiconductor memory device comprising:

a substrate having electrical circuitry formed thereon;

a nanotube connected substantially orthogonal to the substrate;

a conductive ring about the exterior of the nanotube, the conductive ring providing electrical connection from the nanotube to the electrical circuitry on the substrate; and

wherein the nanotube forms a cell of a capacitor and a channel of a transistor.

2. (withdrawn) The device of claim 1 wherein, the nanotube is a carbon nanotube.

3. (withdrawn) A memory cell comprising:

a vertical transistor including a gate, source, drain, and channel wherein a nanotube forms the channel; and

a capacitor.

4. (withdrawn) The device of claim 3 wherein, the nanotube is a carbon nanotube.

5. (withdrawn) The device of claim 3 wherein, the nanotube forms a cell of the capacitor.

6. (withdrawn) The device of claim 4 further including a capacitor ground cell plate formed on the nanotube.

7. (withdrawn) A memory cell comprising:

a vertical transistor having about a 6 kohm connection resistance, the vertical transistor including a gate, source, drain, and channel, wherein a nanotube forms the channel; and

a capacitor, wherein the nanotube forms a cell of the capacitor.

8. (withdrawn) A DRAM cell comprising:

a vertical transistor including a gate, source, drain, and channel wherein a nanotube forms the channel; and

a capacitor having a ground plate, an insulator, and a charge plate wherein the nanotube forms the charge plate.

9. (withdrawn) The device of claim 8 wherein, the gate comprises a conductive ring about an insulated exterior section of the nanotube.

10. (withdrawn) The device of claim 8 wherein, the source comprises a conductive ring about the exterior of the nanotube.

11. (withdrawn) The device of claim 10 wherein, the source directly, physically contacts the nanotube.

12. (withdrawn) The device of claim 8 wherein, the nanotube is substantially orthogonal to a substrate upon which the device is formed.

13. (withdrawn) The device of claim 8 wherein, the nanotube is a carbon nanotube.

14. (withdrawn) A vertical transistor in a memory cell device, the vertical transistor comprising:

a substrate;

a nanotube connected substantially orthogonal to the substrate;

a source and drain formed on the substrate;

a conductive ring formed about an insulated exterior section of the nanotube, the conductive ring forming the gate of the vertical transistor; and

wherein the nanotube forms a channel of the vertical transistor.

15. (withdrawn) The device of claim 14 wherein, the memory cell device includes a capacitor having a capacitor cell formed by the nanotube and the nanotube is formed of carbon.

16. (withdrawn) A memory cell capacitor comprising:

a substrate having a first surface defining a plane;

a nanotube connected substantially vertically to the substrate in relation the plane;

a ground cell plate formed on an exterior wall of the nanotube; and

wherein the nanotube forms a cell of the capacitor.

17. (withdrawn) A semiconductor device comprising:

a substrate having a first surface;

an insulator formed on the first surface of the substrate;

a nanotube connected substantially perpendicular to the substrate;

alternating layers of insulative material, and conductive material formed about an exterior wall of the nanotube, wherein the conductive layers form gates for multiple transistors; and

wherein the nanotube forms an interconnection between the gates of the multiple transistors.

18. (withdrawn) A semiconductor device having an electrical interconnect comprising:

a substrate having a first surface defining a plane;

a first trace formed on a portion of the substrate;

a nanotube having a first end connected to the first trace, the nanotube being substantially vertical in relation to the plane defined by the first surface of the substrate;

a second trace connected to a second end of the nanotube; and

wherein the nanotube forms an electrical connection between the first trace and the second trace.

19. (withdrawn) The device of claim 18 wherein, the nanotube has about a 6 kohm resistance between the first trace and the second trace.

20. (withdrawn) The device of claim 18 further comprising plural nanotubes.

21. (original) A method of making a semiconductor device comprising:

providing a substrate;

forming a first insulation layer on the substrate;

forming a nucleation layer on the first insulation layer;

patterning the nucleation layer to cover the nucleation layer such that portions of the nucleation layer remain exposed;

forming nanotubes on the exposed portions of the nucleation layer, the nanotubes oriented to be substantially vertical in relation to the substrate;

forming an insulative layer over exterior walls of the nanotubes;

forming rings of conductive material about the exterior walls of the nanotubes; and

forming a second insulation layer over the exterior walls of the nanotube.

22. (original) A method of making an electrical interconnect in a semiconductor device comprising:

providing a substrate having a first trace layer;

forming a nucleation layer on the substrate;

patterning the nucleation layer such that a portion of the nucleation layer remains exposed;

forming a nanotube on the exposed portion of the nucleation layer, the nanotube having a lower end connected to the first trace layer;

forming an oxide layer over exterior walls of the nanotube and over the nucleation layer;

patterning the oxide layer to expose an upper end of the nanotube; and

forming a second trace layer such that the upper end of the nanotube is connected thereto.

23. (withdrawn) A semiconductor device comprising:

a transistor including a source, a drain, a gate and a channel;

a capacitor including a source, a gate, and a cell;

a single carbon nanotube connected to the source and drain to form the channel of the transistor and the cell of the capacitor.

24. (withdrawn) A semiconductor device comprising:

a substrate;

a first insulation layer formed on the substrate;

a nanotube connected substantially orthogonal to the first insulation layer;

a first conductive ring encircling a first end of the nanotube, the first conductive ring providing electrical connection from the nanotube to the substrate;

a second insulation layer formed on the first conductive ring;

a second conductive ring formed about an insulated exterior section of the nanotube, the second conductive ring electrically connected to the substrate;

a third insulation layer formed on the second conductive ring;

a third conductive ring encircling a second end of the nanotube, the third conductive ring providing electrical connection of the second end of the nanotube to the substrate; and a fourth insulation layer formed over the third conductive ring.

25. (withdrawn) The device of claim 24, wherein the nanotube comprises a carbon nanotube.

26. (withdrawn) A semiconductor device comprising:

a substrate;

a first insulation layer formed on the substrate;

a nanotube connected substantially orthogonal to the first insulation layer;

a first conductive ring encircling and physically contacting an exterior wall of a first end of the nanotube, the first conductive ring providing electrical connection from the nanotube to the substrate;

a second insulation layer formed on the first conductive ring;

a second conductive ring encircling a first insulated exterior section of the nanotube, the second conductive ring electrically connected at a first end to the substrate;

a third insulation layer formed on the second conductive ring;

a third conductive ring encircling and physically contacting a second insulated exterior section of the nanotube, the third conductive ring electrically connected at a first end to the substrate;

a fourth insulation layer formed on the third conductive ring;

a fourth conductive ring encircling and physically contacting an exterior wall of a second end of the nanotube, the fourth conductive ring providing electrical connection of the second end of the nanotube to the substrate; and

a fifth insulation layer formed on the fourth conductive ring.

27. (withdrawn) The device of claim 26, wherein the nanotube comprises a carbon nanotube.

28. (withdrawn) A semiconductor device comprising:

a substrate;

a first insulation layer formed on the substrate;

a nanotube connected substantially orthogonal to the first insulation layer;

a first conductive ring encircling and physically contacting an exterior wall of a first end of the nanotube, the first conductive ring providing electrical connection from the nanotube to the substrate;

a second insulation layer formed on the first conductive ring;

a second conductive ring encircling and physically contacting an insulated exterior section of the nanotube, the second conductive ring electrically connected at a first end to the substrate;

a third insulation layer formed on the second conductive layer; and

a conductive layer on the third insulation layer, the conductive layer forming a capacitor ground cell plate, the ground cell plate electrically connected to the substrate.

29. (withdrawn) The device of claim 28, wherein the nanotube comprises a carbon nanotube.

30. (new) The method of claim 21, wherein:

the substrate is patterned with traces of an electrical circuit; and

the nucleation layer is patterned so as to achieve connection of the semiconductor device with at least one trace of the electrical circuit.

31. (new) The method of claim 21, wherein the nanotubes are formed as carbon nanotubes.

32. (new) The method of claim 21, wherein the semiconductor device is made so as to comprise at least one transistor including at least a respective one of said nanotubes and at least one of the rings of conductive material formed about the exterior wall of the respective nanotube.

33. (new) The method of claim 21, wherein the semiconductor device is made so as to comprise at least one capacitor including at least a respective one of said nanotubes.

34. (new) The method of claim 21, wherein the semiconductor device is made so as to comprise at least one memory cell including at least a respective one of said nanotubes.

35. (new) The method of claim 34, wherein the memory cell is made so as to include:

a vertical transistor including a gate, a source, a drain, and a channel formed by at least a portion of the respective nanotube; and

a capacitor.

36. (new) The method of claim 35, wherein the capacitor is made so as to include a cell defined by at least a portion of the respective nanotube.

37. (new) The method of claim 36, wherein the capacitor is made so as to include a ground cell plate formed on the respective nanotube.

38. (new) The method of claim 35, wherein the capacitor is made so as to include a ground plate, an insulator, and a charge plate defined by at least a portion of the respective nanotube.

39. (new) The method of claim 35, wherein:

the capacitor is made so as to include, on an exterior wall of the respective nanotube, a ground cell plate; and

at least a portion of the respective nanotube defines a cell of the capacitor.

40. (new) The method of claim 35, wherein the vertical transistor is formed such that:

the transistor includes a source and a drain formed on the substrate;

at least one of the conductive rings defines a gate of the transistor; and

the respective nanotube defines a channel of the transistor.

41. (new) The method of claim 21, wherein the semiconductor device is made so as to comprise at least one via including at least a respective one of said nanotubes.

42. (new) The method of claim 21, wherein the semiconductor device is made such that at least some of the nanotubes form respective portions of respective circuit elements selected from the group consisting of transistors, capacitors, memory cells, and vias, and combinations thereof.

43. (new) The method of claim 21, wherein:

the semiconductor device is made such that at least one of the nanotubes forms a respective portion of a transistor; and

at least one of the rings formed about the respective nanotube is configured as a gate, source, or drain of the transistor.

44. (new) The method of claim 43, wherein the semiconductor device is made such that at least two of the rings are configured as respective gates of multiple transistors of which the respective nanotube is a portion.

45. (new) The method of claim 21, wherein:

at least one of the nanotubes forms a respective portion of a logic gate; and

at least one of the rings formed about the respective nanotube is configured as an input or output of the logic gate.

46. (new) The method of claim 21, wherein at least one of the nanotubes is formed so as to be a respective portion of a memory cell comprising a transistor and a capacitor.

47. (new) The method of claim 21, further comprising forming, with respect to at least one of the nanotubes, a second set of rings of conductive material about the second insulation layer on the nanotube.

48. (new) The method of claim 47, further comprising:

patterning the second insulation layer to expose a portion of the at least one nanotube; and

forming a third set of rings of conductive material about the nanotube.

49. (new) The method of claim 22, wherein the nanotube is formed as a carbon nanotube.

50. (new) The method of claim 22, wherein the nanotube is formed so as to be substantially orthogonal to the substrate.

51. (new) The method of claim 22, wherein the nanotube is formed substantially parallel to the substrate.

52. (new) The method of claim 22, wherein forming the oxide layer includes forming at least one layer of an integrated circuit of which the semiconductor device is a part.

53. (new) The method of claim 52, wherein the layer of the integrated circuit is connected to the nanotube.

54. (new) The method of claim 52, wherein the nanotube is formed so as to define a via extending from the first trace layer through the integrated-circuit layer to the second trace layer.